Patent claims

1. Electronic component operating with acoustic waves, with a multilayer structure, that comprises
- at least one GDE layer (GDE) and
- at least one piezoelectric layer (PS) located in closed contact with the GDE layer and
- in which a piezoelectric excitation layer (PS, PS1) is provided and is provided with HF electrodes (ES1) to excite acoustic waves,
- in which a piezoelectric tuning layer (PS, PS2) is provided to change the elasticity modulus of the GDE material directly via a mechanical warping, or the combination of the tuning layer (PS, PS2) and the GDE layer (GDE) is provided, and is provided with control voltage electrodes (ES2),
- in which the excitation layer and tuning layer is realized via the at least one piezoelectric layer.

2. Component according to claim 1,
that comprises at least one BAW resonator (Bulk Acoustic Wave resonator), whereby the piezoelectric excitation layer (PS, PS1) is a component part of this resonator.

3. Component according to claim 2,
that comprises an acoustic reflector in which a partial layer of the acoustic reflector (AS) is executed as an electrode layer (ES1, ES2) or as a GDE layer (GDE).

4. Component according to claim 2 or 3,
in which electrodes are provided that serve both as HF electrodes (ES1) to excite bulk acoustic waves and as control voltage electrodes (ES2) to change the elasticity modulus of the GDE material and therewith for frequency tuning of the BAW resonator.

5. Component according to at least one of the claims 1 through 4, that comprises at least one surface wave component, whereby the excitation layer (PS, PS1) forms the piezoelectric substrate of this component.

6. Component according to at least one of the claims 1 through 5, in which the multilayer structure is arranged on a carrier substrate (SU).

7. Component according to claim 5 or 6, in which one of the control voltage electrodes (ES2) is arranged on the surface of the piezoelectric layer (PS, PS1) which bears interdigital transducers and further acoustic structures.

8. Component according to at least one of the claims 1 through 7, in which the GDE layer (GDE) and at least one piezoelectric layer (PS, PS1, PS2) are separated by an electrode layer (ES1, ES2).

9. Component according to at least one of the claims 1 through 8, in which only one piezoelectric layer (PS) is provided that serves both as an excitation layer to excite the acoustic wave and as a tuning layer to mechanically warp the GDE layer.

10. Component according to at least one of the claims 1 through 9, in which the GDE layer (GDE) is arranged between the excitation layer (PS1) and the tuning layer (PS2).

11. Component according to at least one of the claims 1 through 10, in which the GDE layer (GDE) possesses electrically-conductive characteristics and replaces one of the control voltage electrodes (ES2) or – in the FBAR embodiments – one of the HF electrodes (ES1).

12. Component according to at least one of the claims 1 through 11, in which the GDE layer (GDE) and the tuning layer (PS, PS2) are arranged between two control voltage electrodes.

13. Component according to at least one of the claims 1 through 12, in which the excitation layer (PS, PS1) is comprised of a material which is selected from PZT, ZnO, AlN or GaN.

14. Component according to at least one of the claims 6 through 13, in which the carrier substrate (SU) comprises a multilayer structure.

15. Component according to at least one of the claims 6 through 14, in which the carrier substrate (SU) comprises a multilayer structure with at least one integrated, passive or active circuit element.

16. Component according to at least one of the claims 6 through 15, in which at least one discrete, passive or active component is arranged on the top side of the carrier substrate (SU).

17. Component according to at least one of the claims 6 through 16, in which at least one chip component is arranged on the top side of the carrier substrate (SU).

18. Component according to claim 17, in which the chip component is a SAW component.

19. Component according to at least one of the claims 6 through 18, in which at least one passive or active circuit element integrated into the carrier substrate (SU) forms at least one part of an adaptation circuit.

20. Component according to at least one of the claims 6 through 19,

in which at least one passive or active circuit element integrated into the carrier substrate (SU) forms either at least one part of an antenna switch, a diode switch, a high-pass filter, a low-pass filter, a bandpass filter, a band elimination filter, a power amplifier, a diplexer, a duplexer, a coupler, a direction coupler, a balun, a mixer or a storage element.

21. Component according to at least one of the claims 6 through 20, in which at least one discrete passive or active circuit element arranged on the top side of the carrier substrate (SU) forms either at least one part of an antenna switch, a diode switch, a high-pass filter, a low-pass filter, a bandpass filter, a band elimination filter, a power amplifier, a diplexer, a duplexer, a coupler, a direction coupler, a balun, a mixer or a storage element.

22. Component according to at least one of the claims 6 through 21, in which at least one part of an adaptation circuit integrated into the carrier substrate is fashioned as one or more conductor paths for later fine adaptation.

23. Component according to at least one of the claims 1 through 22, in which the carrier substrate (SU) is a multilayer ceramic

24. Component according to at least one of the claims 1 through 23, in which the carrier substrate (SU) is comprised of silicon.

25. Component according to at least one of the claims 1 through 24, in which the carrier substrate (SU) is comprised of an organic material, for example plastic or laminate.

26. Component according to at least one of the claims 1 through 25,

in which both one or more chip components and one or more discrete, passive or active circuit elements arranged on the top side of the carrier substrate (SU) represent SMD elements.

27. Component according to at least one of the claims 1 through 26, in which at least one chip component arranged on the top side of the carrier substrate (SU) is housed.

28. Component according to at least one of the claims 1 through 27. in which at least two chip components arranged on the top side of the carrier substrate (SU) are contained by a common housing.

29. Component according to at least one of the claims 1 through 28, that comprises at least two separately housed chip components on the top side of the carrier substrate (SU).

30. Component according to at least one of the claims 1 through 29, in which at least one of the HF electrodes (ES1) or the control voltage electrodes (ES2) comprises a plurality of layers.